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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YASUSHI KUBOTA and HAJIME WASHIO

Appeal 2009-003807
Application 09/775,167
Technology Center 2600

Before JOHN C. MARTIN, JOSEPH F. RUGGIERO, and THOMAS S. HAHN, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1-25, which are all of the pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Rather than reiterate the arguments of Appellants and the Examiner, we refer to the Appeal Brief (filed July 3, 2008) and the Answer (mailed September 15, 2008) for the respective details. We have considered in this decision only those arguments Appellants actually raised in the Brief. Any other arguments which Appellants could have made but chose not to make in the Brief are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants' Invention

Appellants' invention relates to a shift register circuit that includes a plurality of serially connected register blocks each having a flip-flop operating in synchronism with a clock signal. Further included in the shift register circuit is a transfer gate which controls the clock signal applied to the flip-flops. An input control signal of a register block transfer gate is brought into an on-state only in a specified period during which the flip-flop output of a corresponding register block changes. (*See generally* Spec. 34:1-35:6).

Claim 1 further describes the invention and reads as follows:

1. A shift register circuit provided with a plurality of register blocks each having a flip-flop that operates in synchronization with a clock signal and a transfer gate for controlling the clock signal supplied to the flip-flop,

the plurality of register blocks being serially connected together, and

an input control signal of the transfer gate of a corresponding register block being brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes.

The Examiner's Rejections

The Examiner's Answer cites the following prior art references:

Zenda	US 5,111,190	May 5, 1992
Nakao	US 5,289,518	Feb. 22, 1994
Erhart	US 5,572,211	Nov. 5, 1996
Kawaguchi	US 5,602,561	Feb. 11, 1997

Appellants Admitted Prior Art (AAPA) – appearing at pages 6-9 of the Specification and illustrated in Figures 39 through 41J of the drawings.

Claims 1-5, 14, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Nakao and AAPA.

Claims 6, 9-13, 15-19, and 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Nakao, AAPA, and Erhart.

Claims 7 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Nakao, AAPA, Erhart, and Kawaguchi.

Claims 8 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Nakao, AAPA, Erhart, Kawaguchi, and Zenda.

ISSUE

Based on Appellants' contentions, as well as the findings and conclusions of the Examiner, the pivotal issue before us is whether the Examiner erred in determining that AAPA discloses a shift register circuit in which the control signal of the transfer gate of a corresponding register block is "brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes."

ANALYSIS

Claims 1-5, 14, and 25

With respect to the Examiner's 35 U.S.C. § 103(a) rejection of each of the appealed independent claims 1 and 25, Appellants' arguments focus on the alleged deficiency of the Examiner's proposed combination of Nakao and AAPA in disclosing the claimed feature of a shift register circuit in which the control signal of the transfer gate of a corresponding register block is "brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes." In particular, Appellants contend (App. Br. 4-6) that Figs. 41C and 41D of AAPA indicate that the control signal CTL (Fig. 41C) is not brought into an ON-state only when the output OUT1 (Fig. 41D) changes. Rather, in Appellants' view, Figs. 41C and 41D of AAPA indicate that the control signal CTL1 remains in an ON-state when the output OUT1 of the flip-flop

is active and, therefore, the ON-state is not limited to the time period in which the flip-flop output changes.

We find Appellants' arguments to be not commensurate with the scope of the language of claims 1 and 25 and, thus, unpersuasive. We find nothing in claims 1 and 25 which requires that the ON-state of the control signal is limited to the time period during which the flip-flop output is changing from the inactive to the active state, such as described pages 34-35 of Appellants' Specification and illustrated at Figures 2C and 2D of Appellants' drawings.

To the contrary, we agree with the Examiner (Ans. 10) that claims 1 and 25 require only that the control signal be "brought into" an ON-state only when the flip-flop changes, a feature which is illustrated in Figures 41C and 41D of AAPA. As pointed out by the Examiner, while the control signal CTL1 in AAPA remains in the ON-state during the entire period in which the flip-flop output OUT1 is in the active state (Spec. 7:3-8), this is not precluded by the claim language. We further agree with the Examiner that there is no claimed requirement that the control signal be turned OFF, i.e., brought out of the ON-state, before the flip-flop output changes, or that the control signal change every time the flip-flop output changes.

For the above reasons, we sustain the Examiner's 35 U.S.C. § 103(a) rejection of independent claims 1 and 25, as well as dependent claims 2-5 and 14, not separately argued by Appellants.

Claims 6-13 and 15-24

The Examiner's obviousness rejections of dependent claims 6-13 and 15-24, in which the Erhart, Kawaguchi, and Zenda references are applied in

separate combinations with Nakao and AAPA, are also sustained.[2] Appellants' arguments (App. Br. 6) rely on those made against independent claims 1 and 25, which we have found to be unpersuasive.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1-25 for obviousness under 35 U.S.C. § 103(a).

DECISION

The Examiner's decision rejecting claims 1-25 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(v) (2009).

AFFIRMED

[2] While claims 13, 15, and 16 are not included in the heading of the rejection (Ans. 5) based on the combination of Nakao, AAPA, and Erhart, these claims are addressed in the detailed analysis of the rejection (Ans. 6-7).

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